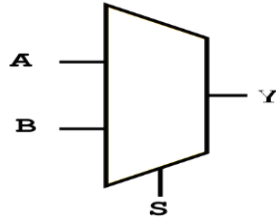# Multiplexer

A multiplexer (mux) is a digital system that selects one out of possible 2^n inputs depending on n select bits. For instance, the truth table and schematic symbol for a 2-to-1 mux are shown below.

symbol of a 2-to-1 mux

And the truth table of (2-to-1) mux is :

S	B	A	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

OR

S	Y
0	A
1	B

The Boolean expression for the output (Y) in terms of inputs A, B and S is:

$$Y = \overline{S}\overline{B}A + \overline{S}BA + SB\overline{A} + SBA$$
$$Y = \overline{S}A(\overline{B} + B) + SB(\overline{A} + A)$$
$$Y = \overline{S}A + SB$$
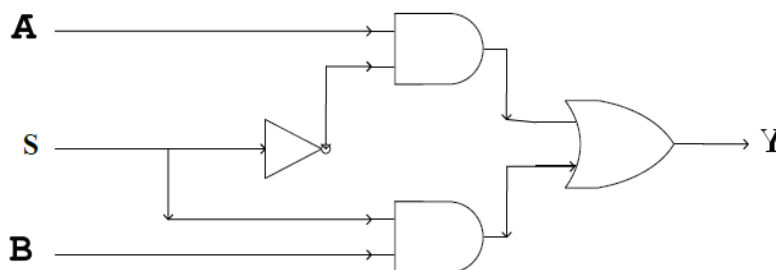
2 - to – 1 multiplexer

Larger multiplexers are also common, if you have 4 inputs then you need 2 select bits. This is the reason for the n-select bits mapping 2^n inputs to one output.

Selectors		Inputs				Output
X	Z	D	C	B	A	Y
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	0
0	0	0	0	1	1	1
0	0	0	1	0	0	0
0	0	0	1	0	1	1
0	0	0	1	1	0	0
0	0	0	1	1	1	1
0	0	1	0	0	0	0
0	0	1	0	0	1	1
0	0	1	0	1	0	0
0	0	1	0	1	1	1
0	0	1	1	0	0	0
0	0	1	1	0	1	1
0	0	1	1	1	0	0
0	0	1	1	1	1	1
0	1	0	0	0	0	0
0	1	0	0	0	1	0
0	1	0	0	1	0	1
0	1	0	0	1	1	1
0	1	0	1	0	0	0
0	1	0	1	0	1	0
0	1	0	1	1	0	1
0	1	0	1	1	1	1
0	1	1	0	0	0	0
0	1	1	0	0	1	0
0	1	1	0	1	0	1
0	1	1	0	1	1	1
0	1	1	1	0	0	0
0	1	1	1	0	1	0
0	1	1	1	1	0	1
0	1	1	1	1	1	1
1	0	0	0	0	0	0
1	0	0	0	0	1	0
1	0	0	0	1	0	0
1	0	0	0	1	1	0
1	0	0	1	0	0	1
1	0	0	1	0	1	1
1	0	0	1	1	0	1
1	0	0	1	1	1	1
1	0	1	0	0	0	0
1	0	1	0	0	1	0
1	0	1	0	1	0	0
1	0	1	0	1	1	0
1	0	1	1	0	0	1
1	0	1	1	0	1	1
1	0	1	1	1	0	1
1	0	1	1	1	1	1
1	1	0	0	0	0	0
1	1	0	0	0	1	0
1	1	0	0	1	0	0
1	1	0	0	1	1	0
1	1	0	1	0	0	0
1	1	0	1	0	1	0
1	1	0	1	1	0	0
1	1	0	1	1	1	0
1	1	1	0	0	0	1
1	1	1	0	0	1	1
1	1	1	0	1	0	1
1	1	1	0	1	1	1
1	1	1	1	0	0	1
1	1	1	1	0	1	1
1	1	1	1	1	0	1
1	1	1	1	1	1	1

x	z	Y
0	0	A
0	1	B
1	0	C
1	1	D

$$Y = \overline{X}\,\overline{Z}A + \overline{X}ZB + X\overline{Z}C + XZD$$
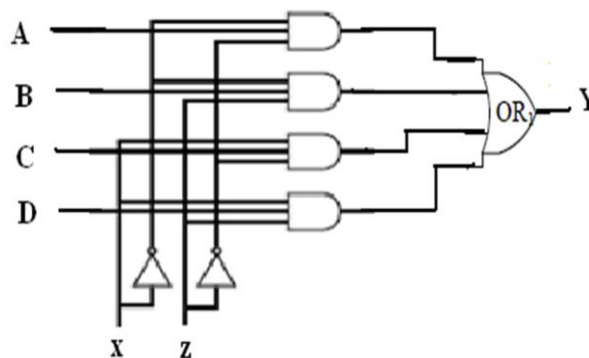
4 - to – 1 multiplexer

Demultiplexer

A demultiplexer basically reverses the multiplexing function. It is take data from one line and distribute them to given number of output lines.
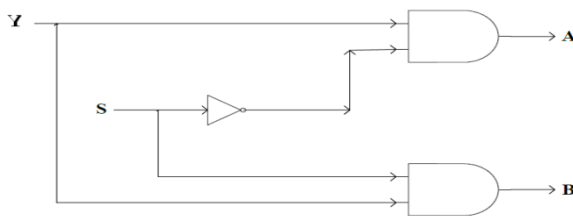
The simplest type of demultiplexer is the 1- to- 2 lines DMUX. as shown in Figure below.

Selector	Input	Outputs	
S	Y	B	A
0	0	0	0
0	1	0	1
1	0	0	0
1	1	1	0

S	A	B
0	Y	0
1	0	Y

$$A = \overline{S}Y$$
$$B = SY$$

1   to 2 Demultiplexer

Figure below   shows a one to four line demultiplexer circuit. The input data line goes to all of the AND gates. The two select lines enable only one gate at a time and the data appearing on the input line will pass through the selected gate to the associated output line.
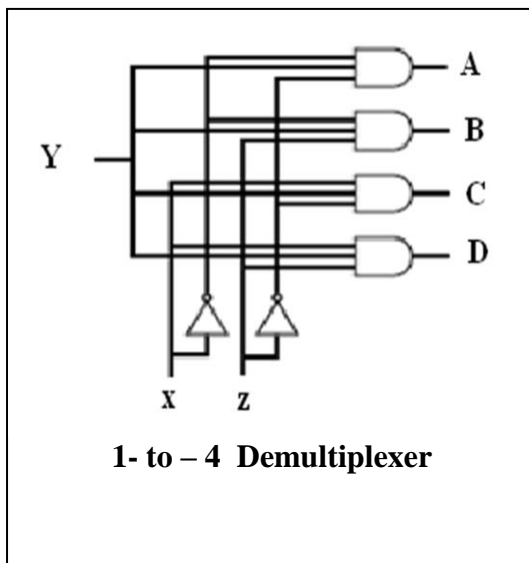
Truth table of 1- to – 4 demultiplexer

X	Z	A	B	C	D
0	0	Y	0	0	0
0	1	0	Y	0	0
1	0	0	0	Y	0
1	1	0	0	0	Y

$$A = \overline{X}\overline{Z}Y$$
$$B = \overline{X}ZY$$
$$C = X\overline{Z}Y$$
$$D = XZY$$

1- to – 4 Demultiplexer